REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated July 12, 2006. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due consideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 2-7 are under consideration in this application. Claim 1 is being cancelled without prejudice or disclaimer. Claims 2-7 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicant's invention.

The claims are being amended to correct formal errors and/or to better recite or describe the features of the present invention as claimed. All the amendments to the claims and the specification are supported by the specification. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Formality Rejection

The drawings were objected to for not showing reference signs described in the specification, and the specification and claims 1-7 were objected to for informalities.

Applicants hereby defer submitting the corrected drawings and the substitute specification until obtaining allowable claims.

Claims 1-7 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite.

Since claim 1 is being cancelled without prejudice or disclaimer and claims 2-7 are being amended as required by the examiner, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Prior Art Rejections

Claims 1-5 were rejected under 35 U.S.C. §102 (e) as being anticipated by US Pat. No. 6,564,367 to Fujii et al. (hereinafter "Fujii"), and claims 6-7 were rejected under 35 U.S.C. §103 (a) as being unpatentable over Fuji in view of US Pat. No. 6,496,886 to Osaka et

al. (hereinafter "Osaka"). These rejections have been carefully considered, but are most respectfully traversed.

The logic verification system of the invention (for example, the embodiment depicted in Figs. 4-6 & 16), as now recited in claim 2, comprises: a logic simulation accelerator including: a logic simulator 0096 operating on a general purpose processor 0013; a device 0007 including a programmable EPGA module 0027 composed by FPGAs (Fig. 16; pp. 35-36); and a bridge circuit 0011 which selectively transmits and receives corresponding data between said logic simulator 0096 operating on said general purpose processor and said FPGA module 0027 according to designed functions assigned to said EPGAs for each of a plurality of designed logic circuits. All pins of the FPGA module 0027 used in a verification process for verifying one of said plurality of designed logic circuits by said logic simulator 0096 are wired in direct to the bridge circuit 0011 to accelerate logic simulation (Fig. 16), a cutting end (e.g., an interface, a port, etc. p. 20, last paragraph) of a verification logic (e.g., Fig. 5) of said one of the plurality of designed logic circuits is assigned to an external interface connector of the FPGA module 0027, and a correspondence between each pin of the external interface connector 0036 of said FPGA module 0027 and a logic signal is established on said logic simulator 0096 on said general purpose processor.

"*The logic simulation accelerator of this embodiment executes the logic simulation program on the disk memory 0014 on the general purpose processor 0013. The bridge circuit 0011 transmits and receives the simulation object logic indicated by hardware on the FPGA and the signal via the general purpose interface to realize the simulation of verification object logic. .... Thereby, the processing rate can be accelerated by reducing the number of processes to be executed with the general purpose processor 0013. The logic simulation accelerator in this embodiment gathers the FPGAs into one module and can be removed at a time* (p. 19, last paragraph)."

Applicants respectfully contend that the cited references do not teach or suggest such "a logic simulator + EPGA module logic verification scheme which including a logic simulation program operating on a general purpose processor working in conjunction with a programmable EPGA module 0027 composed by FPGAs, and a bridge circuit which selectively transmits and receives corresponding data therebetween" as does the invention.

The logical circuit 101 in Fig. 1 of Fujii was relied upon by the Examiner (p. 6, lines 8-9 of the outstanding Office Action) to teach the general purpose processor where the logic simulator (software) resides according to the present invention. However, Fujii's logical

circuit 101 can be any logic circuit (e.g., Fig. 2) to be input into Fujii's logic dividing and module wiring system (Col. 5, lines 50-52) so as to be logically divided into several (e.g., 3) blocks and implemented by three FPGAs (Col. 12, lines 9-11). In other words, Fujii's logical circuit 101 corresponds to a designed logic circuit to be verified by the logic verification system of the invention, rather than any general purpose processor where the logic simulator (software) for simulating designed logic circuits resides inside the logic verification system of the invention. Fuji merely uses a general purpose processor to divide a target logic circuit into different FPGAs, but not to execute a logical simulation on the general purpose processor in conjunction with the FPGA module as the present invention. Therefore, Fujii does not teach such a general purpose processor where the logic simulator (software) for simulating designed logic circuits resides inside the logic verification system of the invention

Moreover, Fujii's switching device in Fig. 3 as relied by the Examiner (p. 6, lines 12-13 of the outstanding Office Action) only provides a physical wiring connection between the FPGAs and connectors, rather than connecting between the EPGA module including EFGAs and a general purpose processor where the logic simulator (software) resides as does the bridge circuit 0011 of the present invention. Therefore, Fujii does not teach such a bridge circuit as in the present invention.

Regarding claim 3, Fujii only considers directions in judging whether the net has diverged, rather than "transmitting a direction control signal of a two-way signal controlled therewith to the bridge circuit using an interface" as does the present invention.

Regarding claim 4, Fujii only recognizes the direction attribute by reading the logic to be verified by the division program that operates on CPU (col. 13, lines 43-45), but not recognizing the direction attribute between said FPGA module and the bridge circuit as does the present invention.

Regarding claim 5, Fujii only uses the priority specification and the timing calculation result by human to obtain the direction attribute acquired according the discussion regarding to claim 4 (col. 5, lines 35-45), rather than automatically detecting the signal direction of the two-way signal by physical signal wave forms.

Regarding claims 6-7, Osaka was relied upon by the Examiner to compensate for Fujii's deficiencies. However, Osaka only teaches a method of wiring for the substrate with directionality couplers on the substrate compared with the bus signal between CPU parts and the memory devices actual. The composition is different from the "logic simulator + EPGA module logic verification scheme of the present invention. Moreover, it only detects the data

transfer error in each connection destination, but not to judge whether the direction attribute is a disagreement as does the present invention.

The cite prior art references and their combinations fail to teach or suggest each and every feature of the present invention as recited in independent claim 2 and it dependent claims. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and telephone number indicated below.

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